What is claimed is:

1. A method for modifying the function of a state machine having a programmable logic device, the method comprising:

(a) modifying a high-level design of said state machine to obtain a modified high-level design of said state machine with a modified function;

(b) generating a programmable logic device netlist from differences in said high-level design and said modified design; and

(c) installing said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist.

2. The method of claim 1, wherein step (b) includes:

extracting a high-level programmable logic device design from said modified high-level design.

3. The method of claim 2, wherein said extracting includes comparing said high-level design to said modified high-level design.

4. The method of claim 2, wherein said generating a programmable logic device netlist includes synthesizing said a high-level programmable logic device design.

5. The method of claim 4, wherein said programming of said programmable logic device includes compiling said programmable logic device into a pattern and applying said pattern to a static random access memory array of an integrated circuit containing said state machine and said programmable logic device.

6. The method of claim 1, further including the step of:

(d) determining if said programmable logic device includes enough gates to program said modified function.

7. The method of claim 1, further including, before step (a) performing a static timing analysis to determine a maximum allowable size for said programmable logic device.

8. The method of claim 6, wherein said performing said static timing analysis is performed on a netlist synthesized from said high-level design of said state machine.

9. The method of claim 1, wherein said high-level design of said state machine is a portion of a high level design of an integrated circuit and said modified high-level design of said state machine is a portion of a modified version of said high level design of said integrated circuit.

10. The method of claim 1, wherein said high-level design of said state machine includes one or more multiplexers for interconnecting said programmable logic device to said state machine.

11. The method of claim 1, wherein said programmable logic device is connectable between a next stage logic and a state latch of said state machine in either a next state path, a current state path or both.

12. The method of claim 1, wherein said programmable logic device is connectable between an input of said state machine, an output of said state machine or both.

13. The method of claim 1, wherein said programmable logic device is adapted to add programmable logic device latch bits to a state latch of said state machine.

14. The method of claim 1, wherein said programmable logic device is shared between said state machine and one or more additional state machines.

15. The method of claim 1, wherein said programmable logic device is selected from the group consisting of programmable read only memories, simple programmable logic devices, programmable array logic devices, generic array logic devices, programmable logic arrays, complex programmable logic devices, erasable programmable logic devices,

electrically-erasable programmable logic devices, multiple array matrices, field programmable interconnect devices, static random access memory based programmable logic devices and antifuse based programmable logic devices.

16. A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for modifying the function of a state machine having a programmable logic device, said method comprising the computer implemented steps of:

(a) modifying a high-level design of said state machine to obtain a modified high-level design of said state machine with a modified function;

(b) generating a programmable logic device netlist from differences in said high-level design and said modified design; and

(c) installing said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist.

17. The system of claim 16, wherein step (b) includes:

extracting a high-level programmable logic device design from said modified high-level design.

18. The system of claim 17, wherein said extracting includes comparing said high-level design to said modified high-level design.

19. The system of claim 17, wherein said generating a programmable logic device netlist includes synthesizing said a high-level programmable logic device design.

20. The system of claim 19, wherein said programming of said programmable logic device includes compiling said programmable logic device into a pattern and applying said pattern to a static random access memory array of an integrated circuit containing said state machine and said programmable logic device.

21. The system of claim 16, further including the step of:

(d) determining if said programmable logic device includes enough gates to program said modified function.

22. The system of claim 16, further including, before step (a) performing a static timing analysis to determine a maximum allowable size for said programmable logic device.

23. The system of claim 21, wherein said performing said static timing analysis is performed on a netlist synthesized from said high-level design of said state machine.

24. The system of claim 16, wherein said high-level design of said state machine is a portion of a high level design of an integrated circuit and said modified high-level design of said state machine is a portion of a modified version of said high level design of said integrated circuit.

25. The system of claim 16, wherein said high-level design of said state machine includes one or more multiplexers for interconnecting said programmable logic device to said state machine.

26. The system of claim 16, wherein said programmable logic device is connectable between a next stage logic and a state latch of said state machine in either a next state path, a current state path or both.

27. The system of claim 16, wherein said programmable logic device is connectable between an input of said state machine, an output of said state machine or both.

28. The system of claim 16, wherein said programmable logic device is adapted to add programmable logic device latch bits to a state latch of said state machine.

29. The system of claim 16, wherein said programmable logic device is shared between said state machine and one or more additional state machines.

30. The system of claim 16, wherein said programmable logic device is selected from the group consisting of programmable read only memories, simple programmable logic devices, programmable array logic devices, generic array logic devices, programmable logic arrays, complex programmable logic devices, erasable programmable logic devices,

electrically-erasable programmable logic devices, multiple array matrices, field programmable interconnect devices, static random access memory based programmable logic devices and antifuse based programmable logic devices.